IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Application of:
Jiaw-Ren Shin

Group Art Unit: 2818

Serial No.: 10/761,658

Examiner: Dang, Phuc T.

Filed: Jan. 20, 2004

In Response to Office Action
Dated: Jan. 13, 2005

For: Deep Well Implant Structure Providing Latch-Up Resistant CMOS Semiconductor Product

Attorney Docket No.: 67,200-1194

Certificate of Mailing

I hereby certify that this paper is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Kathy Dixon

Date: Mar. 11, 2005

RESPONSE TO OFFICE ACTION

Commissioner for Patents
Alexandria, VA 22313-1450

Dear Sir:

In response to an Office Action mailed Jan. 13, 2005 of a restriction requirement imposed by the Examiner, the Applicants hereby elect with traverse the prosecution of Group I, device claims 1-10. Attached is a Petition for Extension of Time, together with a Credit Card Payment form, to extend the reply time to March 13, 2005.